**Project Proposal**



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**CSE-304L Computer Organization & Architecture Lab**

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“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

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Submitted to:

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**Project Proposal:**

**Implementation of SAP-1 in Verilog**

**Problem Statement:**

The current landscape of digital design and computer architecture education lacks comprehensive resources for understanding and implementing the Simple-As-Possible-1 (SAP-1) architecture using Hardware Description Language (HDL) such as Verilog. This project aims to bridge this gap by creating a detailed and practical guide for implementing SAP-1 in Verilog, enabling learners and enthusiasts to gain hands-on experience in digital design.

**Project Description:**

This project involves the implementation of SAP-1 using Verilog, a hardware description language widely used for digital design. The goal is to create a comprehensive and accessible resource that guides users through the entire process of designing, simulating, and synthesizing the SAP-1 architecture.

**Steps Of Implementation Method:**

**1. Research and Understanding:**

**a.** Conduct an in-depth study of the SAP-1 architecture, including its components and functionalities.

**b.** Explore existing resources and implementations of SAP-1 in other languages to gather insights.

**2. Verilog Environment Setup:**

**a.** Set up the development environment with the necessary Verilog tools and simulators.

**b.** Ensure compatibility with popular Verilog synthesis tools.

**3. Register Design**:

**a.** Define and implement the registers of the SAP-1 architecture.

**b.** Verify the functionality through simulation, ensuring proper data storage and retrieval.

**4. Arithmetic and Logic Unit (ALU):**

**a.** Design the ALU based on the specifications of SAP-1.

**b.** Implement arithmetic and logic operations and validate through simulation.

**5. Memory Unit:**

**a.** Define the memory unit and its addressing mechanisms.

**b.** Implement read and write operations and verify through simulation.

**6. Control Unit:**

**a.** Develop the control unit responsible for orchestrating the operation of the SAP-1.

**b.** Implement instruction decoding and sequencing logic.

**7. Integration and Testing:**

**a.** Integrate all components and verify the overall functionality of the SAP-1.

**b.** Conduct extensive testing and debugging to ensure the correctness of the design.

**8. Documentation:**

a. Create comprehensive documentation explaining the Verilog implementation of SAP-1.

b. Include clear diagrams, code explanations, and simulation results.

**9. Educational Materials:**

**a.** Develop supplementary educational materials such as tutorials, presentations, and examples.

**b.** Provide guidance on how learners can experiment with and expand upon the SAP-1 implementation.

**10. Expected Outcome:**

The project aims to produce a robust Verilog implementation of the SAP-1 architecture, accompanied by detailed documentation and educational materials. The outcome will serve as a valuable resource for individuals seeking hands-on experience in digital design and computer architecture, enhancing their understanding of fundamental concepts.

**Project Summary:**

The Simple-As-Possible-1 (SAP-1) architecture is a minimalist and educational computer architecture designed to teach the fundamentals of computer organization and architecture. The SAP-1 architecture consists of a set of registers, arithmetic and logic units (ALU), control unit, and memory, providing a solid foundation for understanding the principles of digital systems. Implementing SAP-1 in Verilog will contribute to the educational landscape by providing a practical and accessible guide for learners and enthusiasts. The project aligns with the goal of demystifying digital design and fostering a deeper understanding of computer architecture.